

# A 2W, 65% PAE SINGLE-SUPPLY ENHANCEMENT-MODE POWER PHEMT FOR 3V PCS APPLICATIONS

*Der-Woei Wu, Ray Parkhurst, Shyh-Liang Fu, John Wei, Chung-Yi Su\*, Shih-Shun Chang, Dennis Moy, Wesley Fields, Patrick Chye, Rich Levitsky*

*Communication Semiconductor Solutions Division, \*HP Laboratories, Palo Alto, CA. Hewlett-Packard Company, Newark, CA 94560.*

## Abstract

An enhancement-mode power PHEMT process has been developed for low-voltage wireless subscriber power amplifier applications. Employing a highly selective reactive ion etching process to define the vertical position of the Schottky gate, this device only requires a positive voltage. A 12-mm gate periphery device demonstrated 33dBm output power (167mW/mm), 14.7dB power gain (16.7dB linear gain), and 65.4% PAE at 3V and 1.8GHz.

## I. Introduction

The critical demands of low cost, light weight, low supply voltage, and long battery lifetime for the emerging PCS/PCN markets have placed stringent requirements for the selection of power devices. Pseudomorphic high electron mobility transistors (PHEMTs) have been thought to be a key device for portable applications due to their high gain, high power density, and superior efficiency at low drain bias [2-5]. In this paper, we describe the fabrication and characterization of an enhancement-mode power PHEMT (E-PHEMT) for 3V PCS applications. This device technology is differentiated from the depletion-mode devices and other device technologies by the following unique features. Firstly, it only requires a positive voltage and has a very low drain current with zero volts on the gate, which simplifies the bias circuitry, and eliminates the noise associated with generating a negative voltage. Secondly, the inherent high transconductance at low quiescent current due to accurate gate placement close to the channel has led to more ideal class-B operation and exhibited better transconductance linearity as well as excellent power added efficiency. Thirdly, low knee voltage, low on-resistance (high mobility), high

breakdown voltage and high current carrying capability (double-doped channel) due to optimal profile design make this device extremely suited for high gain, high power density, and high efficiency power amplification at a low supply bias.

## II. Device Technology and Fabrication

Figure 1 shows the epitaxial structure of the developed PHEMT grown by molecular beam epitaxy (MBE). The active part of the epitaxial structure consists of an undoped InGaAs (25% In) channel layer sandwiched by two n-type AlGaAs donor layers. A heavily doped n<sup>+</sup> GaAs cap layer was grown on the top of an undoped AlGaAs layer to provide good ohmic contacts.

Device fabrication employs highly selective reactive ion etching (RIE) to define the vertical position of the Schottky gate. After proton implant isolation, the power PHEMTs are fabricated by a standard FET process. This consists of Au/Ge/Ni ohmic contacts, Ti/Pt/Au gate, plasma SiN passivation, and TiW/Au interconnect metal. The Schottky gate is placed on the top of undoped AlGaAs layer after selectively removing the top n<sup>+</sup> GaAs cap layer by RIE.

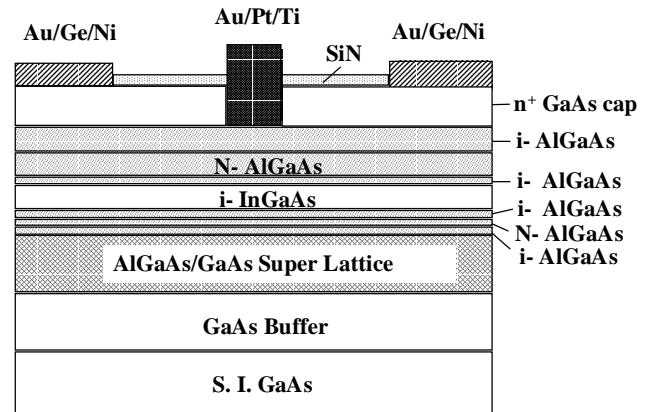


Figure 1. Cross section of the E-PHEMT.

### III. Device Performance

#### PCM Device Performance

The current-voltage (I-V) characteristics of a 60 $\mu\text{m}$  ( $L_g=0.5\mu\text{m}$ ) double-doped E-PHEMT is shown in Figure 2. The device shows good pinch-off characteristics even at high drain bias. Typical DC results were summarized in Table 1. The high values of  $I_{\text{max}}$  and  $g_m$  as well as the low knee voltage and on-resistance are attributed to the double-doped channel and the optimal designed structure.

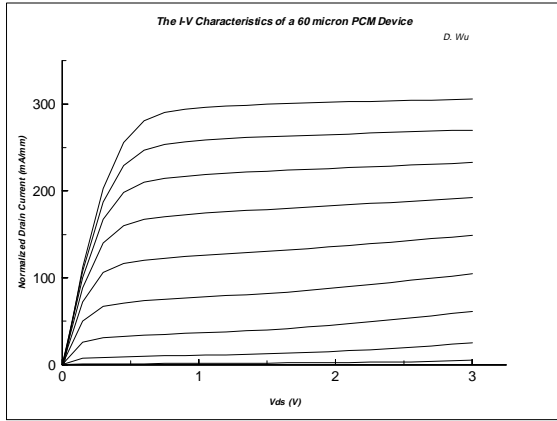


Figure 2 The I-V characteristics of a 60 $\mu\text{m}$  PCM device. The  $V_{\text{gs}}$  starts at 0V (bottom curve) and stops at +0.8V (top curve) with a step of +0.1V.

Table 1 Typical DC Characteristics.

Parameter	Measured Condition	Value
$I_{\text{dss}}$	$V_{\text{ds}}=3\text{V}$ , $V_{\text{gs}}=0\text{V}$	$<10\text{mA/mm}$
$I_{\text{max}}$	$V_{\text{ds}}=3\text{V}$ , $V_{\text{gs}}=0.8\text{V}$	$>300\text{mA/mm}$
Max. $g_m$	$V_{\text{ds}}=3\text{V}$	$>400\text{mS/mm}$
$BV_{\text{gdo}}$	$I_g<0.5\text{mA/mm}$	$>10\text{V}$
$V_k$	$I_{\text{ds}}=200\text{mA/mm}$ , $V_{\text{gs}}=0.8\text{V}$	0.3V
$R_{\text{on}}$	$V_{\text{ds}}/I_{\text{ds}}$ with $V_{\text{gs}}=0.8\text{V}$	1.5ohm-mm

The small-signal parameters of the 300 $\mu\text{m}$  devices were measured on-wafer using an HP8510C automated network analyzer. Based on the S-parameter results, the unity current-gain frequency ( $f_T$ ) for  $V_{\text{ds}}=3\text{V}$  and  $I_{\text{ds}}=20\text{mA}$  are calculated to be 36GHz. The maximum available gain/maximum stable gain (MAG/MSG) at 2GHz is 22dB under the same bias condition.

The large-signal performance of the PCM devices was also monitored on-wafer using an ATN automatic load-pull system. The large-signal characteristics were measured at  $V_{\text{ds}}=3\text{V}$

and  $I_{\text{ds}}=20\text{mA}$ . With a fixed input power, the system sets the input tuner impedance to provide maximum small-signal gain, and then tunes the load impedance for maximum gain, maximum power, and maximum efficiency. The power saturation characteristics for a 300 $\mu\text{m}$  device under the maximum output power tuning is shown in Figure 3. The device exhibited an output power of 16.4dBm at the 3dB gain compression point with 3 volts bias at 2GHz. In addition, the device demonstrated a saturated output power of 18dBm, PAE of 60%, and power gain of 13dB, which corresponds to a power density of 210mW/mm.

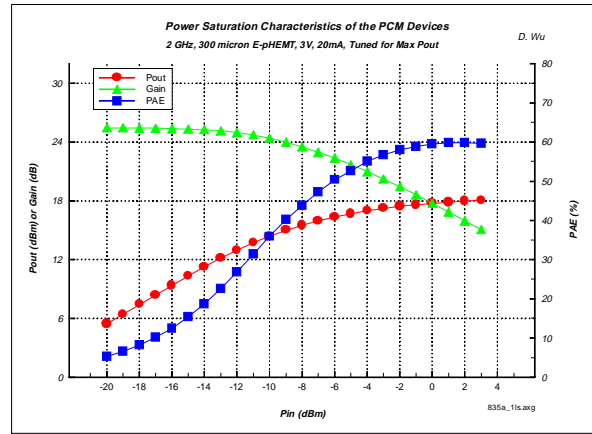


Fig. 3 The power saturation characteristics of the 300 $\mu\text{m}$  PCM device at 3V and 2GHz.

#### 12mm Device Performance

The power device used in this work is a 0.5 $\mu\text{m}$  gate length and 12mm (36-finger) gate periphery enhancement-mode PHEMT. The photograph of the device is shown in Figure 4. The power performance of a 12mm E-PHEMT was measured with a drain bias of 3V and a quiescent drain current of 100mA at 1.8GHz. To improve yield and reduce cost, the wafer has no via grounding. The device was eutectically mounted onto a metal carrier, and two ceramic probe adapters, which provide the coplanar-to-microstrip transition, were then placed at the input and output of the device. Bond wires were used to connect the gate and drain metallization to the adapter microstrip. Several bond wires were also bonded from the source pads down to

the ground metallization to ensure low ground inductance.

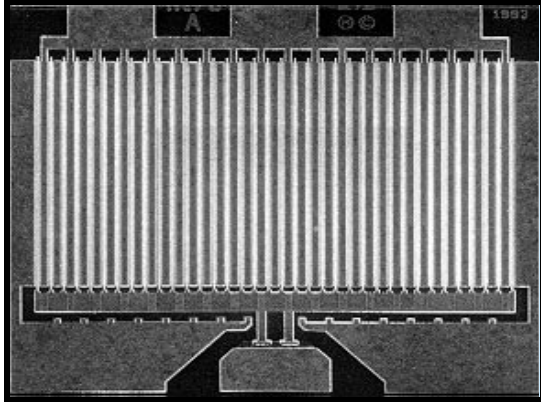


Figure 4 The photograph of a 12mm power device.

The power characteristics were measured using a vector-corrected active load-pull system [1]. The use of active load-pull system ensures that sufficiently low impedance is presented to the device for optimal performance. In addition, it also provides the capability to study the effects of harmonic tuning on power performance. Figure 5 shows the power saturation characteristics for the 12mm device under maximum power tuning.

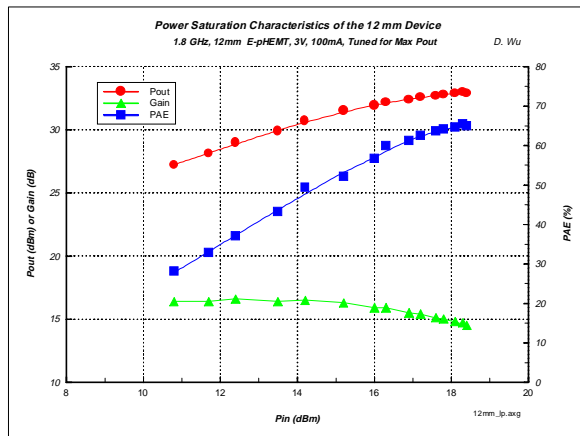


Figure 5 The power saturation characteristics for the 12mm device at 3V and 1.8GHz.

The results were obtained with both fundamental and second harmonic tuning. The improvement in PAE by terminating the second harmonics is about 4-6%. At 1.8GHz, the 12mm device achieved 33dBm output power (corresponding to a power density of 167mW/mm), 14.7dB power gain (2dB gain compression), and

65.4% PAE at 3V, which is believed to be the highest combined power performance ever reported at such a low bias at 1.8GHz.

#### State-of-the-Art Performance Comparison

To benchmark the performance, results obtained above are compared with several competing technologies used in similar applications. The power performance (in terms of the power density) of the E-PHEMT is compared with several state-of-the-art depletion-mode PHEMT devices operating in the 3V range (Figure 6). It is noted that several results were reported at 900MHz range. Also, most of the depletion-mode devices require dual-supply as opposed to the single-supply in our case. In addition, Table 2 compares our 12 mm E-PHEMT device performance with high-performance MESFETs, high-performance Si BJT, GaAs/AlGaAs HBTs, Si LDMOS, and SiGe HBTs.

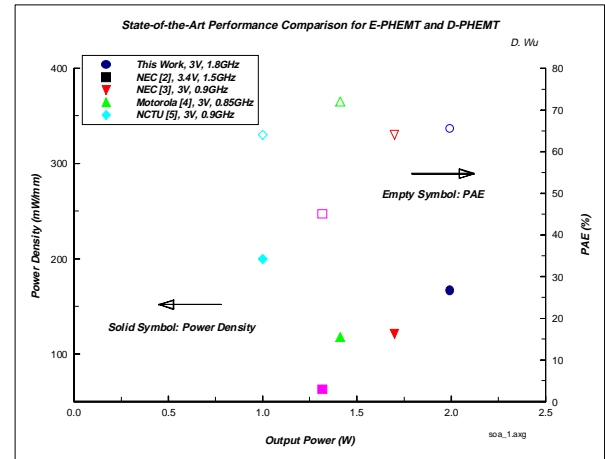


Figure 6 Power performance comparison of state-of-the-art PHEMT in the 3V range.

Table 2 Power performance comparison for several competing technologies used in portable wireless applications.

Freq(GHz)	Pout(dBm)	PAE(%)	Vs(V)	Device Technology
1.8	33	65.4	3	This Work
1.9	30	44	4.7	SiGe HBT [6]
1.8	24	60	3.5	Double-poly Si BJT [7]
0.9	31.3	68	2.3	Hi-Lo MESFET [8]
0.93	32.8	71	3.5	MESFET, 2fo Tuning [9]
1.9	22.6	69	3	GaAs/AlGaAs HBT [10]
1.88	33	70	5	GaAs/AlGaAs HBT [11]
1.9	24.7	54	3.3	BPLDD SAGFET [12]
1.5	30.4	48	3.5	Delta-doped MESFET [13]
0.85	31.8	65	5.8	Si LDMOS [14]

#### IV. Conclusion

An enhancement-mode power PHEMT process has been developed for low-voltage wireless applications. A 12-mm device achieved 2W output power, 14.7dB power gain, and 65.4% PAE at 3V and 1.8GHz, which is the highest power performance among competing device technologies. The ability of operating at single power supply and demonstrating excellent power performance at a low bias voltage makes this E-PHEMT very suitable for power generation in portable wireless applications.

#### V. Acknowledgment

Special thanks are due to Alex Cognata for performing the active load pull measurement and Brian Hughes (both at HP MWTD, Santa Rosa) for stimulating discussions of active load pull measurement results. The authors would also like to acknowledge the personnel at HP Labs for initial device and process development and the personnel at CSSD GaAs foundry for device fabrication.

#### References

- [1]. B. Hughes, A. Ferrero, A. Cognata, "Accurate On-Wafer Power and Harmonic Measurements of mm-Wave Amplifiers and Devices," *IEEE MTT-S Digest*, pp. 1019-1022, 1992.
- [2]. Y. Hasegawa, Y. Ogata, I. Nagasako, K. Inosako, N. Iwata, M. Kanamori, and T. Itoh, "3.4V Operation Power Amplifier Multi-Chip IC's for Digital Cellular Phone," *IEEE GaAs IC Symp. Dig.*, pp. 63-66, 1995.
- [3]. K. Inosako, K. Matsunaga, Y. Okamoto, and M. Kuzuhara, "Highly Efficient Double-Doped Heterjunction FET's for Battery-Operated Portable Power Applications," *IEEE EDL-15.*, pp. 248-250, 1994.
- [4]. V. Nair, S. Tehrani, D. Halchin, E. Glass, E. Fisk, and M. Majerus, "High Efficiency Power HFETs for Low Power Wireless Applications," *IEEE MMWCS Digest*, pp. 17-20, 1996.
- [5]. Y.-L. Lai, E. Chang, C.-Y. Chang, T. K. Chen, T. H. Liu, S. P. Wang, T. H. Chen, and C. T. Lee, "5mm High-Power-Density Dual-Delta-Doped Power HEMT's for 3V L-Band Applications," *IEEE EDL-17.*, pp. 229-231, 1996.
- [6]. A. Schüppen, S. Gerlach, H. Dietrich, D. Wandrei, U. Seiler, and U. König, "1-W SiGe Power HBT's for Mobile Communication," *IEEE MWGW Lett.*, pp. 341-343, 1996.
- [7]. M. Versleijen, R. Dekker, W. v. d. Einde, and A. Pruijmboom, "Low-Voltage High-Performance Silicon RF Power Transistors," *IEEE MTT Symp. Dig.*, pp. 563-566, 1995.
- [8]. J.-L. Lee, J. K. Mun, H. Kim, J.-J. Lee, and H.-M. Park, "A 68% PAE, GaAs Power MESFET Operating at 2.3V Drain Bias for Low Distortion Power Applications," *IEEE Trans. on ED, Vol. 43, No. 4*, pp. 519-526, 1996.
- [9]. M. Maeda, H. Takehara, M. Nakamura, Y. Ota, and O. Ishikawa, "A High Power and High Efficiency Amplifier with Controlled Second-Harmonic Source Impedance," *IEEE MTT Symp. Dig.*, pp. 579-582, 1995.
- [10]. Y. Matsuoka, S. Yamahata, M. Nakatsugawa, M. Muraguchi, and T. Ishibashi, "High-Efficiency Operation of AlGaAs/GaAs Power Heterojunction Bipolar Transistors at Low Collector Supply Voltage," *Electron. Lett.*, pp. 982-984, 1993.
- [11]. P. Walters, P. Lau, K. Buehring, J. Penney, C. Farley, P. McDade, and K. Weller, "A Low Cost Linear AlGaAs/GaAs HBT Power Amplifier with Active Bias Sensing for PCS Applications," *IEEE GaAs IC Symp. Dig.*, pp. 67-70, 1995.
- [12]. N. Kasai, M. Noda, K. Ito, K. Yamamoto, K. Maemura, Y. Ohta, T. Ishikawa, Y. Yoshii, M. Nakayama, H. Takano, and O. Ishihara, "A High Power and High Efficiency GaAs BPLDD SAGFET with WSi/W Double-Layer Gate for Mobile Communication System," *IEEE GaAs IC Symp. Dig.*, pp. 59-62, 1995.
- [13]. S. Makioka, S. Enomoto, H. Furukawa, K. Tateoka, N. Yoshikawa, and K. Kanazawa, "A Miniaturized GaAs Power Amplifier for 1.5GHz Digital Cellular Phones," *IEEE MMWCS Digest*, pp. 13-16, 1996.
- [14]. D. Ngo, C. Dragon, J. Costa, D. Lamey, E. Spears, and W. Burger, "RF Silicon MOS Integrated Power Amplifier for Analog Cellular Applications," *IEEE MTT-S Digest*, pp. 559-562, 1996.